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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,754	10/30/2003	Victor Chan	FIS920030191 (00750480AA)	6186

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EXAMINER	
DANG, TRUNG Q	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 12/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/695,754	CHAN ET AL.	
	Examiner	Art Unit	
	Trung Dang	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *12-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of the Group II, claims 1-11 in the reply filed on 9/22/04 is acknowledged. The traversal is on the ground(s) that has not made a prima facie demonstration of distinctness and that a serious burden must be made to support a requirement for restriction. This is not found persuasive because of the followings:

A) While the examiner agrees with applicants that the showing of distinctness in the previous restriction requirement is in error because the examiner's proposal of materially different process falls within the scope of claim 1, the distinctness between method claims and device claims can still be shown as follows:

a) The process as claimed can be used to make other and materially different product, for example, the claimed process could be used to made a metal wiring structure having reduced stress in a selected portion, or

b) Alternatively, the product as claimed can be made by another and materially different process, for example, the first layer (or the second layer) having a first stress level in a first region and a second stress level in a second region could be formed by selectively thinning the first layer (or the second layer) located in the first region while keeping the first layer (or the second layer) located in the second region intact.

B) As for applicants' argument that serious burden has not been made, this is found unconvincing because the issues of product and method claims are divergent. There may be some overlap in the searches of the two groups, but there is no reason to believe that the searches would be identical. Furthermore, the examination of the process claims is based on different criteria from that of the device claims, hence the examination of the two groups is not co-extensive. Therefore, based on the additional work involved in searching and examination of the two distinct inventions together that would present serious burden to the examiner, restriction of distinct invention is clearly proper.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 8, 9, and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Kumagai et al. (US 2004/0075148).

Since claim 1 does not require the first layer of material is different from the second layer of material, a single layer of material could be broadly interpreted as consisting of a first layer corresponds to a lower portion and a second layer corresponds to an upper portion. In this regard, the reference anticipates the claims in that it discloses a method of adjusting carrier mobility for different semiconductor conductivities on the same chip comprising the steps of:

forming NMOS transistor **10** and PMOS transistor **30** on the same substrate (Fig. 11 and para. [0197]);

forming a stress control film **191** of silicon nitride (SiN) providing tensile stress on a portion of a surface of the substrate (Fig. 12, para. [0198]. Note that the stress control film **191** corresponds to the claimed first and second layer for the reason set forth above, and hence the tensile stress of the film corresponds to the claimed first and second stress level)

selectively implanting ions of Si, Ge, N, O, or Ar into a portion of the stress control film **191** covering the PMOS transistor, thereby selectively reducing the stress level of said portion from tensile to compressive (Fig. 13 and para. [0202]-[0203]).

3. Claims 1-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Huang et al. (US 2004/0104405).

With reference to Figs. 1-4, the reference anticipates the claimed invention in

that it discloses a method of adjusting carrier mobility for different semiconductor conductivities on the same chip comprising the steps of:

forming NMOS transistor **12** and PMOS transistor **14** on the same substrate;

forming a first layer **40** of SiN or SiON providing a compressive stress on the NMOS and PMOS portions of the substrate (Fig. 1 and para. [0026]);

selectively reducing said compressive stress of a portion of said first layer **40** by selectively removing the portion covering the NMOS transistor (Fig. 2);

forming a second layer **50** of SiN or SiON providing a tensile stress on the NMOS and PMOS portions of the substrate (Fig. 3 and para. [0034]);

selectively reducing said tensile stress of a portion of said second layer **50** by selectively removing the portion covering the PMOS transistor (Fig. 4).

Note that when a portion of a stress layer is removed, the stress level corresponding to that portion is reduced from compressive (or tensile) to non-existent.

As for claim 2, the claimed limitation is met when the tensile stress layer **50** is interpreted as the first layer and the compressive stress layer **40** is interpreted as the second layer.

For claims 3-8, see paragraphs [0048] to [0053] for the teaching that the first layer **40** is formed by PECVD and paragraph [0043] for the teaching that the second layer **50** is formed by thermal CVD.

For claim 10, see Fig. 3.

4. Claims 1-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Chidambarrao et al. (US 2004/0113217)

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

With reference to Figs. 4a-4b, the reference anticipates the claimed invention in that it discloses a method of adjusting carrier mobility for different semiconductor conductivities on the same chip comprising the steps of:

forming NFET and PFET on the same substrate (step 1 in Fig. 4a);

forming a compressive SiN layer providing a compressive stress on the NFET and PET portions of the substrate (step 3 in Fig. 4a));

selectively reducing said compressive stress of a portion of said compressive SIN by selectively removing the portion covering the NFET (step 5 in Fig. 4a);

forming a tensile SiN layer providing a tensile stress on the NFET and PET portions of the substrate (step 7 in Fig. 4b);

selectively reducing said tensile stress of a portion of said tensile SiN layer by selectively removing the portion covering the PMOS transistor (step 9 in Fig. 4b).

Note that when a portion of a stress layer is removed, the stress level corresponding to that portion is reduced from compressive (or tensile) to non-existent.

For claims 2-8, see paragraph [0027].

For claim 10, see step 7 in Fig. 4b.

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claim 1 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 8 of copending Application No. 10/318,602 to Chidambarrao et al. cited above. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 8 of the copending application includes limitations of claim 7, hence the selective removal of the first spacer material and the second spacer material selectively reduces the first type of mechanical stress and the second type of mechanical stress, respectively, to non-existent.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trung Dang whose telephone number is 571-272-1857. The examiner can normally be reached on Mon-Friday 9:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trung Dang
Primary Examiner
Art Unit 2823

10/23/04